

Finding Power/Ground Defects on Connectors - A New Approach

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Abstract

Printed circuit boards are steadily becoming faster, and as a result, relatively ordinary defects in connectors and sockets can now have more subtle and damaging effects. At the same time these defects defy detection by conventional technologies. This paper surveys existing tests for these defects and introduces a new solution based on Network Parameter Measurements.

1 Introduction

A paper given at the 2005 International Test Conference discussed High-Speed Signal Propagation (HSSP) and how boards that support such technology are becoming commonplace in the electronics industry [Park05]. Board designers will need to study HSSP design (see [JoGr03]) in order to know what new design techniques will be needed. Suddenly, boards must have well-controlled characteristic impedances which imply strict layout rules. Even such mundane concepts as the design of a via have new engineering considerations. Multiple power and ground pins on ICs (already common today) will continue to be important, and not simply for the mitigation of ground-bounce. Certain “mundane” devices such as bypass capacitors must now be chosen with care, and their placement becomes a critical design problem. Simple connectors and sockets are no longer “simple”. They become something more like a waveguide as frequency and data rate rise [TTI06]. Through-hole attachments common for sockets and connectors will be forced to change to ball-grid attachments.

Moore’s law allows us to pack more of a system into an IC, and it also allows us to package capabilities that can be used to change the architecture of a system such that we can achieve new heights of performance. For example, Serialize/Deserialize technology (SerDes) was once used in high-end systems to form high-speed serial links between subsystems. Now we can pack multiple SerDes channels (both transmit and receive) into a single IC and use them to transmit serialized data with embedded clocking between ICs on a single board. This new architecture is replacing parallel buses that needed separate clock distribution systems with complex skew control. SerDes technology is now becoming prevalent in low-end consumer products. PCI-Express [PCIE07] in the

personal computer world is a prime example of this trend. The first wave of this standard started with serial data rates of 2.5 Gigabits/second, and will move up to 5, maybe someday even 10 Gbps.

2 Connector and Socket Defects

The [Park05] paper examined the effects of open ground pins in connectors. For example, a typical PCI Express connector is shown in Figure 1.

PCI Express x4 Connector Top View

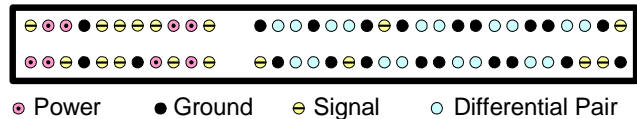


Figure 1: PCI Express pin assignments.

This connector has 29 pins of the 64 total pins that are *not* devoted to signaling, but are there to provide power and ground connections. Of these 29 pins, 18 are devoted to creating HSSP signal return paths, and are ground pins found on the right-hand side of the keyway. The other 11 pins on the left-hand side of the keyway are devoted to supplying power current at several different voltages. The signal return path ground pins are essential to the design of the board, to assure signal integrity of the high-speed differential data signal pairs. If there is a continuity problem on a signal return ground pin, then several problems may result.

1. Loss of signal integrity margin.
2. Increased Bit Error Rate.
3. Increased Electromagnetic Interference (EMI).

Board designers create circuits with some level of signal margin to assure that by the time a signal propagates from its source to its destination, there is sufficient signal still present to reliably transfer information. Every physical feature in that path is considered for its potential to degrade signal margins, from IC pins, to bends and corners in traces, to vias between layers, and connectors in the pathway. An additional defect on a signal return path may add unanticipated signal margin degradation. If a connector was (for example) rated to drive a USB cable of several different lengths, the defect might hamper the use of a 3

meter cable, but a 1 meter cable might still have sufficient signal margin to operate correctly.

Decreased signal margin may lead to increased probability of bit errors in an HSSP signal stream. This increase could be catastrophic and obvious, or it could be much more subtle, with errors occurring sporadically and apparently at infrequent, random intervals. These are the types of errors most likely to escape.

Finally, discontinuities in a signal return path caused by a continuity defect will have the effect of increasing the loop area of the current that is traveling in the signal return path. This can create a virtual antenna that may then radiate radio frequency energy that is unanticipated by the designer. This energy may be transmitted to other parts of the local circuitry causing local interference, or, may escape to the outside world where it may cause difficulties with meeting regulatory requirements for EMI compliance.

The [Park05] paper looked predominantly at two-row connectors such as PCI Express or DDR2 styles. However, sockets that house ICs are basically multi-row connectors that possess this same problem with open pins on signal return paths. When boards containing sockets and connectors are manufactured, the mating ICs or connectors (typically) are *not* present during testing. This leads to a discussion of how these devices could be tested.

3 Traditional Testing for Opens Coverage

There are several ways to approach the testing of connectors and sockets. There are two inspection approaches and In-Circuit test.

3.1 Inspection

If a socket or connector uses through-hole technology for board mounting, then an automatic optical inspection (AOI) test may be capable of finding opens on connector pins. Pins protruding from the bottom of the board can be inspected for presence (they were not bent during insertion) and for the existence of solder. As attachment technology proceeds to surface-mount schemes, AOI may no longer be possible.

That leaves automatic X-Ray inspection (AXI) as a possible approach. Penetrating radiation can see surface-mount attachments and inspect for the quality of soldering.

Either inspection technique could require a new test step in an assembly line that was not there before. This means reconfiguring the line, buying the equipment and considering the throughput rate of this equipment. In some cases the throughput of AXI systems is less than needed and this (or its cost) may prevent its use.

3.2 In-Circuit Test

In-Circuit test (ICT) has been a popular approach for testing sockets and connectors, but it has its limitations.

There are two approaches: contact test via mated connections, and non-contact sensing.

3.2.1 Mated Connections

It is possible to build a test fixture that provides for the insertion of mating connectors into the connectors-under-test. The mating connectors have a harness of wiring that brings each pin's signal (or ground/power potential) back to the tester where it can be monitored. Here there are two approaches: have a human operator insert each connector mate, or have pneumatic mechanisms automatically insert the mating connectors. The former is potentially time-consuming and error-prone while automatic mating systems are expensive to create and maintain, and may potentially damage board connectors that have minor seating or alignment problems. Neither approach is very popular for these reasons.

Note that an IC socket could be tested in a similar way. However a socket may have 700 or more pins in a small area, so its wiring harness would be very dense and fragile at the same time. Then there is the question of how to depress the mating unit into the socket when the harness is in the way. One approach around this problem is to build a special test IC that has the same mechanical form-factor as the intended IC, but contains special circuitry to support the testing of the socket. This approach is used in industry in higher volume applications that can justify the high expense of creating a dedicated test device. This device is likely to be unique to a given socket and its connectivity to a board, so whenever either changes the special IC may need to be redesigned, at significant cost. Consider also that many sockets have lids and spring-clips that have to be opened before the test device can be inserted and then closed. This implies human handling during the test.

3.2.2 Non-Contact Sensing

Over a decade ago, a test technology known generically as "Capacitive Leadframe Testing" [Turn96] and in the industry as "TestJet" was developed for unpowered testing for open signal pins on ICs¹. The technique was soon extended for testing signal pin opens on connectors and sockets as well as depicted in Figure 2. The ICT has access to the signals attached to the connector pins. All but the pin-under-test are grounded and the tested pin is stimulated with an AC signal. A sense plate is suspended above the connector so that there is a small capacitive coupling between the tip of each pin in the connector to the sense plate. (The sense plate is not inserted into the connector.) A defect-free pin will couple its AC signal into the sense plate where a buffer boosts the signal and sends it to the tester. If there is an open

¹ "TestJet" is a registered trademark of Agilent Technologies.

between the connector pin and board, then the AC signal is significantly attenuated as seen at the sense plate, indicating a defect.

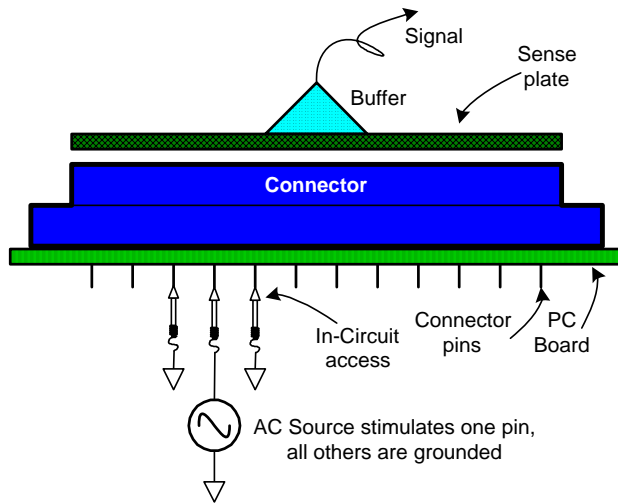


Figure 2: The basic TestJet setup for testing connector pins for opens.

TestJet-style testing of connectors will find open defects on signal pins in the connector, but it is largely ineffective on “fixed” pins such as power and ground pins. This is because of two reasons:

1. Redundant pins
2. Bypass capacitance

Take the case of the PCI Express connector in Figure 1. There are 21 pins all connected to the same node (ground). If we were to place our AC source on the ground node and guard all the other pins to ground, then we would have 21 pin tips coupled to the sense plate. This would give a strong signal, but the variability of the coupling might produce a +/-10% reading from board to board. If one pin (of the 21) was open, then we would expect a reading that might be low by about 5%. This would not be reliably visible and we would most likely get false passes for open defects on ground pins. But the second reason also plays havoc with this measurement: There are 8 power pins in this connector, and almost certainly, each is bypassed to the ground node with a large capacitance. This capacitance is designed to damp out noise between power and ground, and our test setup is trying to inject a signal between these nodes. Thus, our AC source will struggle to create a signal in the presence of this large capacitance, which appears as an AC short across the power and ground nodes. This will frustrate taking a valid measurement. Thus, today at ICT we have little recourse but to accept poor open pin coverage on connectors and sockets when these devices have populations of pins connected to ground and power nodes.

3.3 Functional Test

There is one other opportunity to test for open power/ground pins in connectors and sockets and this is during functional test. Functional test often occurs in a dedicated area after In-Circuit test, but before final system integration. “Hot Mockups” are often used to house a board, where it can receive power and interact with whatever backplanes, cables and plug-in boards it might encounter in real life. In this environment, special diagnostic routines are exercised that *may* stimulate any hidden defects still within the board. As reported in [Park05] it is possible that an open ground pin in a connector or socket could pass these functional tests and ultimately be shipped. If indeed a functional test does show a failure for this type of defect, the question becomes, where is the defect? Diagnostic resolution may be quite poor during this type of testing, leading to an inventory of suspect boards that cannot be easily fixed.

4 A New Approach

Here we introduce a new approach to finding open power and ground pins on sockets and connectors, at In-Circuit test. This approach uses the exact same setup as seen in Figure 2 since it is based on the TestJet paradigm. However, there is where similarity ends. The new technique is named “Network Parameter Measurement” or NPM for short.

4.1 Background

Consider a simple two-row connector. Physically it is constructed as an insulating housing containing two rows of identical pins, locked into place. (See Figure 3.)

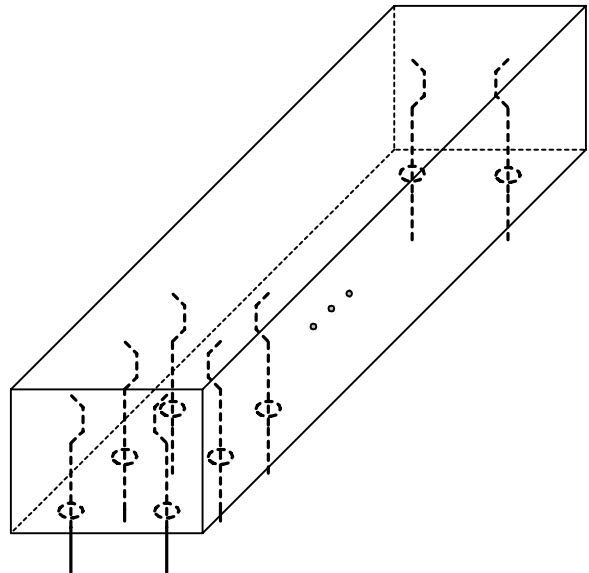


Figure 3: View of a typical two-row connector.

However, for higher frequency applications, there is more to the connector than just the mechanical aspects.

The electrical characteristics are also critical. If you contact the support organization of a connector vendor, you can ask for an electrical model of the connector. This is usually documented in the form of a Spice description, and it can be surprisingly detailed. Indeed, a “simple” DDR2 model supplied to us consisted of over 2,000 lines of Spice code. The point of this is there are important electrical characteristics of the pins *and their relationship to each other* that are carefully specified and engineered.

When you analyze the model of the DDR2 connector, you see that each pin has four main electrical components, a series resistance, a series inductance, capacitance to neighboring pins, and mutual inductance with neighbors. This can be conceptualized in Figure 4 for just a group of four pins. The inter-pin capacitances are shown in blue and the mutual inductances are indicated by red loops.

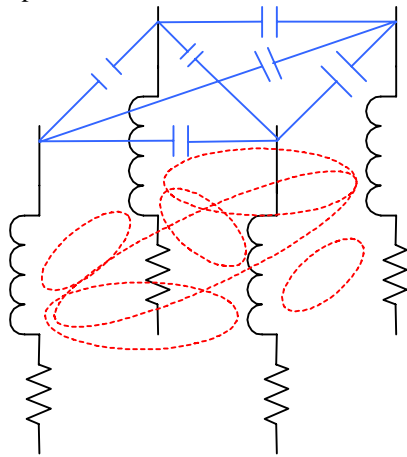


Figure 4: Electrical model of a group of 4 pins.

These relationships will exist between any group of four neighboring pins in this connector, and weaker coupling will exist between pins that are farther away, although these more distant relations quickly become less important. The values of these “components” are measured in milliohms, nanohenrys and femtofarads, but are quite important to the high-frequency behavior of the connector.

4.2 Network Parameter Measurement

When a sense plate is stationed over the connector, there is a capacitance from each pin tip to the sense plate. These are also small-valued capacitances and the resultant circuit looks like that in Figure 5.

To analyze the effects of defects, it is instructive to look at a much simpler case such as a two pin connector with one signal and one ground pin, as seen in Figure 6. In this configuration, we have the left-hand side of the parallel structure stimulated by the tester’s signal source, while the right-hand side is connected to the board’s (and tester’s) ground plane. Now, in the design of connectors, the values of $R_{Series1}$ and $R_{Series2}$, and also $L_{Series1}$ and

$L_{Series2}$, will be substantially equal. The value of C_{Couple} in this case is unique, although in larger connectors there will be many such capacitances which will vary depending on surrounding neighborhood effects.

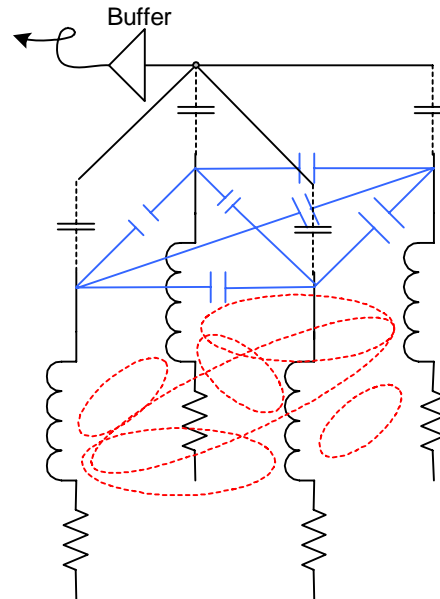


Figure 5: A four-pin group coupled to a sense plate and buffer.

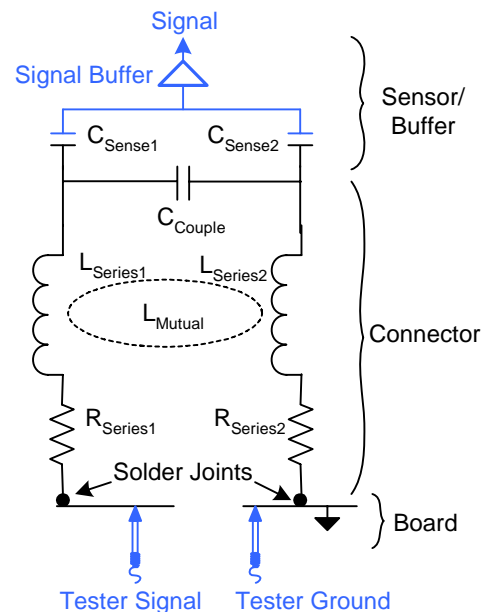


Figure 6: Simple case: A signal pin next to a ground pin, with no pin defects present.

The presence of the sense plate mounted above the connector will give rise to new capacitances C_{Sense1} and C_{Sense2} . Again, the values of these capacitances may be substantially equal, or may be somewhat different, again due to neighborhood effects. For example, pins near the

end of a large connector may have different C_{Sense} values compared to those seen in more crowded interior regions

In the no-defect case, we are stimulating the left-hand side with a low-impedance source. The series resistance and series inductance together contribute a series impedance that may attenuate the signal somewhat by the time it gets to the branch of C_{Sense1} and C_{Couple} capacitors. On the right-hand side, we see a similar series impedance that is connected between ground and another C_{Sense2} and C_{Couple} branch. The values for all these series components are relatively low, so we see a lot of tester stimulus on the left-hand side and on the right-hand side we see very little signal. (The signal lost via the mutual inductance is also relatively low.) Thus most of the signal coupled into the sense plate comes from C_{Sense1} and that becomes our reading for a defect-free connector.

Now consider a defect that opens the joint of the signal pin in the simple two-pin connector, as shown in Figure 7. This defect modifies the circuit to inject C_{Open} in series with $R_{Series1}$ and $L_{Series1}$. This significantly reduces the amount of signal coupled into the left-hand leg of the circuit and the branch where C_{Couple} intersects the signal drains off much of its magnitude. Thus we see a much-reduced reading at the sense plate.

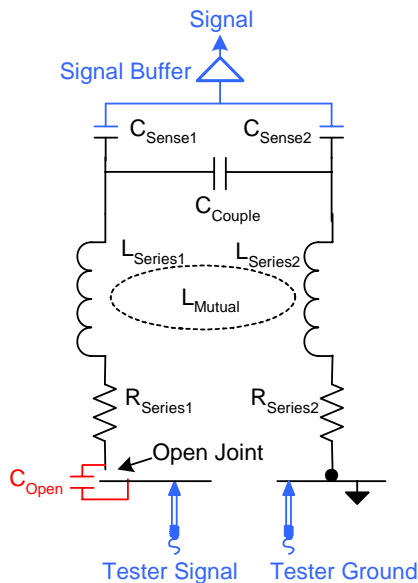


Figure 7: A model for the case where the signal pin is open and detectable.

Next, consider the case where the ground pin is open due to a solder defect, for example. This case is shown in Figure 8. Now we have an interesting case where instead of a low-impedance ground on the right-hand side, we have injected C_{Open} in series, which changes the effect of C_{Couple} significantly. Now, some of the signal energy in the left hand leg is transferred to the right-hand leg where C_{Sense2} can transmit it to the sense plate buffer. Depending on the various circuit element values, the buffer will see a

signal that is larger than the good-circuit case. In some cases, it may indicate a value approaching twice the normal reading. So we have this result: a “normal” reading indicates no defect is present. A low reading indicates that the signal pin is open, and a high reading indicates the ground pin neighboring the signal pin is open.

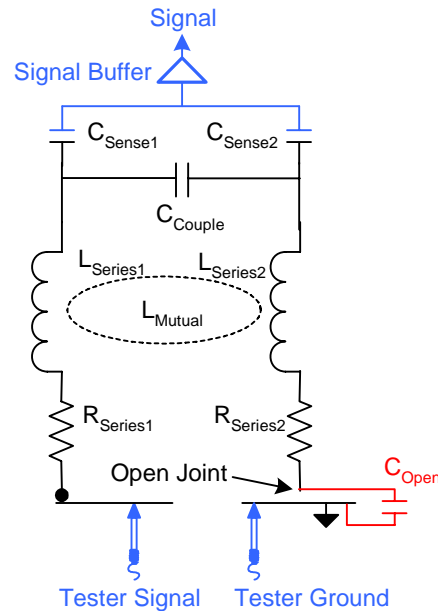


Figure 8: A model for the case where the ground pin is open and detectable.

Finally, consider the case where a ground pin is open but isolated from the signal pin by another ground as may be the case when power and grounds are clustered together. This case is shown in Figure 9.

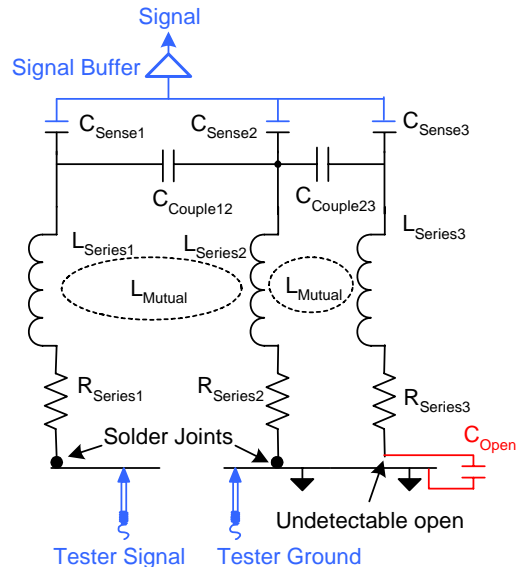


Figure 9: A model for the case where a ground pin is open but undetectable.

As in the no-defect case energy transferred from the left-hand leg to the center leg is dissipated to ground and little of the energy is transferred to the right-hand leg. Thus most of the signal coupled into the sense plate comes from C_{Sense1} and our reading is not differentiable from a defect-free connector. Therefore this defect case is not detectable.

The two-pin and three-pin connectors have illustrated the general concept. When larger connectors are tested, we must account for more parallel paths, but the idea is the same.

5 Experimental Results

Several experiments have been performed to see if NPM technology provides usable, reliable results. Figure 10 shows one example of a production board that was seeded with three connector opens.

The NPM test was run and a failure ticket resulted (see Figure 11). The first indicated open is on a power node and the subsequent two were for ground pins, of which each connector had many.

Notice that the report calls out “Possible Opens”. This is because NPM technology sometimes over-reports opens when indeed, some do exist. When an open does exist, the change in measured network parameters may indicate the actual open, but may not be able to determine exactly which pin is open. All possible opens are indicated including those that are not really there, but could have been. This is arguably a “false fail”, but it only occurs in certain topologies where a real defect is present but there is some ambiguity in locating it. The board will have to be repaired in any case which is certainly preferable to shipping a defect.

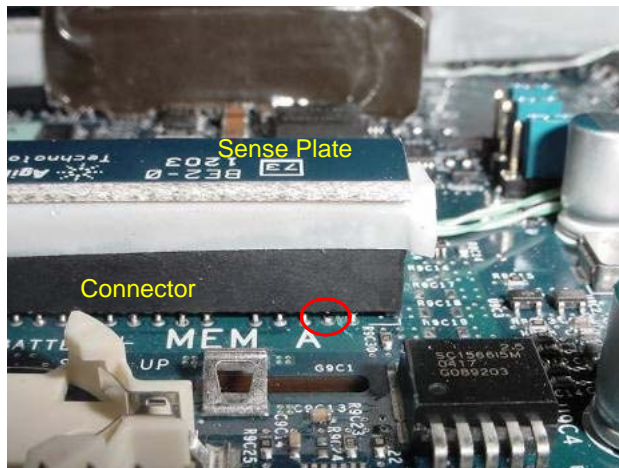


Figure 10: A connector on a board with an open pin defect created by a broken pin (red circle).

A larger scale analysis was done to determine how board-to-board and fixture-to-fixture variations affect the measurements. For example, small mechanical mounting variations between board and connector can cause tilting

or tipping of the socket or connector off-level. Fixture mechanics can result in sense plate alignment variations from board to board. These can cause deviations in measured readings that must be compensated for.

```
-----
Board Name: C05-MB C51896_004
Board Version: **BASE**
Thu May 12 13:56:30 2005
-----
```

```
<NPM REPORT>
DEVICE j9c3 POSSIBLE OPENS:
  Pin A4  Node: IMI_C_P12V
-----
```

```
<NPM REPORT>
DEVICE j7a2 POSSIBLE OPENS:
  Pin A4  Node: GND
-----
```

```
<NPM REPORT>
DEVICE j3d1 POSSIBLE OPENS:
  Pin 237 Node: GND
-----
```

Figure 11: NPM test failure ticket for 3 opens on power and ground pins.

In order for an NPM test to differentiate between the no-defect case and the defect case illustrated in Figure 8, the effect of C_{Sense2} on the sensor plate must be significantly greater than the board to board and fixture to fixture variations of the measurement. Analysis of data from approximately 100,000 pins on a variety of connectors, fixtures, and board types taken from a manufacturing environment showed that the effect of C_{Sense2} was more than three times the standard deviation of the measured value of C_{Sense1} . This empirical data has shown that with appropriate selection of limits, greater than 80% of open grounds can be detected with a false call rate of less than one pin in 10,000.

In another analysis, a “typical” server board was analyzed for coverage. On this board were four large CPU sockets and thirteen connectors of varying types, from DDR2 to PCI Express. The total pin count of the sockets and connectors was 4513, of which 2266 (50%) were power and ground. The analysis showed that 1994 (88%) of these power and ground pins were testable. This included all the connector pins, but 292 power/ground pins in the sockets (73 in each) were not visible with NPM technology. This is due to ground pin clustering that shields some ground pins from observation, as motivated in Figure 9. This can lead to some fairly simple DFT rules for laying out power and grounding in IC ball arrays, which are the driver for this reduction in coverage. This will require cooperation with IC package designers who define the distribution of power and ground pins ultimately seen in sockets. To summarize, we achieved 100%

open pin coverage in the connectors, and 94% coverage in the sockets where before, 50% was our best case.

The speed of the testing was commensurate with the TestJet use-model as well. NPM tests do take longer because more analysis of data is needed, but then again, much more is being tested. We found a 15% increase in test time on a typical connector when we began to include power and ground pins, which nearly doubled the pin coverage. We believe we can further optimize the test time in the future.

6 Conclusion

With the spread of high-speed designs into common products, we are entering a new era where untested defects of the past are increasingly important to future product quality. In this defect class are opens on power and ground pins in sockets and connectors. Network Parameter Measurement technology, based on the familiar TestJet use-model, can provide coverage for these defects during In-Circuit testing. NPM technology offers significant new coverage at In-Circuit test that was previously impractical to enjoy.

7 Acknowledgements

The authors would like to acknowledge valuable contributions to the development of NPM technology made by Rod Browen, Chris Jacobsen, Myron Schneider and Eddie Williamson.

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